

## ABSTRACT OF THE DISCLOSURE

A semiconductor memory device with low power consumption in driving control signals of shift registers.

5 The device contains a plurality of memory cell arrays each composed of a predetermined number of rows of memory cells. One set of shift registers are coupled to each cell array, and the nth set of shift registers successively activate word line selection signals according to a given control

10 signal, so that the corresponding word lines of the nth cell array will be refreshed. Also coupled to each cell array is a shift register controller. The nth shift register controller provides a control signal to the nth set of shift registers when the nth cell array is being

15 refreshed. When the refresh of that cell array is finished, the nth shift register controller forwards the control signal to the (n+1)th set of shift registers, thus initiating refresh operation for the (n+1)th cell array.

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